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Inventor Name Search Result

Your Search was:

Last Name = DORIS
First Name = BRUCE

Application#	Patent#	Status	Date Filed	Title	Inventor Name 51
10876873	Not Issued	020	06/25/2004	LOW-GIDL MOSFET STRUCTURE AND METHOD FOR FABRICATION	DORIS, BRUCE B.
10872605	Not Issued	020	06/21/2004	HYBRID SUBSTRATE TECHNOLOGY FOR HIGH-MOBILITY PLANAR AND MULTIPLE-GATE MOSFETS	DORIS, BRUCE B.
10862073	Not Issued	020	06/04/2004	STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES	DORIS, BRUCE B.
10830347	Not Issued	020	04/22/2004	STRAINED SILICON CMOS ON HYBRID CRYSTAL ORIENTATIONS	DORIS, BRUCE B.
10793084	Not Issued	030	03/04/2004	AMORPHOUS AND POLYCRYSTALLINE SILICON NANOLAMINATE	DORIS, BRUCE B.
10751831	Not Issued	071	01/05/2004	STI STRESS MODIFICATION BY NITROGEN PLASMA TREATMENT FOR IMPROVING PERFORMANCE IN SMALL WIDTH DEVICES	DORIS, BRUCE B.
10732322	Not Issued	030	12/10/2003	SECTIONAL FIELD EFFECT DEVICES AND METHOD OF FABRICATION	DORIS, BRUCE B.
10725849	Not Issued	030	12/02/2003	ULTRA-THIN SI CHANNEL MOSFET USING A SELF-ALIGNED OXYGEN IMPLANT AND DAMASCENE TECHNIQUE	DORIS, BRUCE B.
10725848	Not Issued	030	12/02/2003	ULTRA-THIN SI MOSFET DEVICE STRUCTURE AND METHOD OF MANUFACTURE	DORIS, BRUCE B.

10722873	Not Issued	041	11/26/2003	STRUCTURE AND METHOD TO FABRICATE FINFET DEVICES	DORIS, BRUCE B.
10717737	Not Issued	020	11/20/2003	DUAL GATE FINFET	DORIS, BRUCE B.
10711200	Not Issued	019	01/01/0001	MULTI-GATE DEVICE WITH HIGH K DIELECTRIC FOR CHANNEL TOP SURFACE	DORIS, BRUCE B.
10711182	Not Issued	019	01/01/0001		DORIS, BRUCE B.
10710277	Not Issued	020	06/30/2004	STRUCTURE AND METHOD FOR MANUFACTURING PLANAR SOI SUBSTRATE WITH MULTIPLE ORIENTATIONS	DORIS, BRUCE B.
10710273	Not Issued	020	06/30/2004	ULTRA THIN BODY FULLY-DEPLETED SOI MOSFETS	DORIS, BRUCE B.
10710272	Not Issued	019	01/01/0001	METHOD AND STRUCTURE FOR STRAINED FINFET DEVICES	DORIS, BRUCE B.
10709314	Not Issued	030	04/28/2004	METHOD FOR FORMING NARROW GATE STRUCTURES ON SIDEWALLS OF A LITHOGRAPHICALLY DEFINED SACRIFICIAL MATERIAL	DORIS, BRUCE B.
10709248	Not Issued	030	04/23/2004	STRUCTURE AND METHOD OF MANUFACTURING A FINFET DEVICE HAVING STACKED FINS	DORIS, BRUCE B.
10709239	Not Issued	030	04/23/2004	STRUCTURES AND METHODS FOR MANUFACTURING OF DISLOCATION FREE STRESSED CHANNELS IN BULK SILICON AND SOI CMOS DEVICES BY GATE STRESS ENGINEERING WITH SIGE AND/OR SI:C	DORIS, BRUCE B.
10709129	Not Issued	030	04/15/2004	METHODS FOR MANUFACTURING A FINFET USING A CONVENTIONAL WAFER AND APPARATUS MANUFACTURED THEREFROM	DORIS, BRUCE B.

10708451	Not Issued	030	03/04/2004	PLANAR PEDESTAL MULTI GATE DEVICE	DORIS, BRUCE B.
10708430	Not Issued	030	03/03/2004	MOBILITY ENHANCED CMOS DEVICES	DORIS, BRUCE B.
10708378	Not Issued	030	02/27/2004	HYBRID SOI/BULK SEMICONDUCTOR TRANSISTORS	DORIS, BRUCE B.
10707878	Not Issued	030	01/20/2004	POLYCRYSTALLINE SILICON LAYER WITH NANO-GRAIN STRUCTURE AND METHOD OF MANUFACTURE	DORIS, BRUCE B.
10707840	Not Issued	020	01/16/2004	PROTECTING SILICON GERMANIUM SIDEWALL WITH SILICON FOR STRAINED SILICON/SILICON GERMANIUM MOSFETS	DORIS, BRUCE B.
10707690	Not Issued	030	01/05/2004	STRUCTURES AND METHODS FOR MAKING STRAINED MOSFETS	DORIS, BRUCE B.
10707018	Not Issued	030	11/14/2003	STRESSED SEMICONDUCTOR DEVICE STRUCTURES HAVING GRANULAR SEMICONDUCTOR MATERIAL	DORIS, BRUCE B.
10701526	Not Issued	030	11/06/2003	HIGH MOBILITY CMOS CIRCUITS	DORIS, BRUCE B.
10695748	Not Issued	030	10/30/2003	STRUCTURE AND METHOD TO ENHANCE BOTH NFET AND PFET PERFORMANCE USING DIFFERENT KINDS OF STRESSED LAYERS	DORIS, BRUCE B.
10682430	Not Issued	041	10/10/2003	HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER	DORIS, BRUCE BENNETT
10669727	Not Issued	071	09/25/2003	FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME	DORIS, BRUCE B.
10663471	Not Issued	030	09/15/2003	SELF-ALIGNED PLANAR DOUBLE-GATE PROCESS BY SELF-ALIGNED OXIDATION	DORIS, BRUCE B.
10650229	Not Issued	030	08/28/2003	ULTRA THIN CHANNEL MOSFET	DORIS, BRUCE B.
10605889	Not Issued	041	11/04/2003	OXIDATION METHOD FOR ALTERING A FILM	DORIS, BRUCE B.

				STRUCTURE AND CMOS TRANSISTOR STRUCTURE FORMED THEREWITH	
10604190	Not Issued	041	06/30/2003	HIGH PERFORMANCE CMOS DEVICE STRUCTURES AND METHOD OF MANUFACTURE	DORIS, BRUCE B.
10318600	Not Issued	041	12/12/2002	ISOLATION STRUCTURES FOR IMPOSING STRESS PATTERNS	DORIS, BRUCE B.
10314499	6667197	150	12/06/2002	METHOD FOR DIFFERENTIAL OXIDATION RATE REDUCTION FOR N-TYPE AND P-TYPE MATERIALS	DORIS, BRUCE B.
10301436	6686637	150	11/21/2002	GATE STRUCTURE WITH INDEPENDENTLY TAILORED VERTICAL DOPING PROFILE	DORIS, BRUCE B.
10212938	Not Issued	093	08/05/2002	METHOD FOR BLOCKING IMPLANTS FROM THE GATE OF AN ELECTRONIC DEVICE VIA PLANARIZING FILMS	DORIS, BRUCE B.
10195596	6657244	150	06/28/2002	STRUCTURE AND METHOD TO REDUCE SILICON SUBSTRATE CONSUMPTION AND IMPROVE GATE SHEET RESISTANCE DURING SILICIDE FORMATION	DORIS, BRUCE B.
10160540	6709926	150	05/31/2002	HIGH PERFORMANCE LOGIC AND HIGH DENSITY EMBEDDED DRAM WITH BORDERLESS CONTACT AND ANTISPACER	DORIS, BRUCE BENNETT
10078779	6562713	150	02/19/2002	METHOD OF PROTECTING SEMICONDUCTOR AREAS WHILE EXPOSING A GATE	DORIS, BRUCE B.
10015239	6613602	150	12/13/2001	MONOLITHICALLY INTEGRATED COLD POINT THERMOELECTRIC COOLER	DORIS, BRUCE BENNETT
10000695	6509221	150	11/15/2001	METHOD FOR FORMING HIGH PERFORMANCE CMOS DEVICES WITH ELEVATED SIDEWALL SPACERS	DORIS, BRUCE B.
09938097	6642147	150	08/23/2001	METHOD OF MAKING THERMALLY STABLE PLANARIZING FILMS	DORIS, BRUCE B.
09905233	6566210	150	07/13/2001	METHOD OF IMPROVING GATE ACTIVATION BY	DORIS, BRUCE B.

				EMPLOYING ATOMIC OXYGEN ENHANCED OXIDATION	
09902830	6512266	150	07/11/2001	METHOD OF FABRICATING SIO2 SPACERS AND ANNEALING CAPS	DORIS, BRUCE B.
09888160	6531365	150	06/22/2001	ANTI-SPACER STRUCTURE FOR SELF-ALIGNED INDEPENDENT GATE IMPLANTATION	DORIS, BRUCE B.
09882250	6586289	150	06/15/2001	ANTI-SPACER STRUCTURE FOR IMPROVED GATE ACTIVATION	DORIS, BRUCE B.
09864974	6645867	150	05/24/2001	STRUCTURE AND METHOD TO PRESERVE STI DURING ETCHING	DORIS, BRUCE B.
09841531	Not Issued	161	04/24/2001	FORMATION OF NOTCHED GATE USING A MULTI-LAYER STACK	DORIS, BRUCE B.

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Last Name = DORIS
First Name = BRUCE

Application#	Patent#	Status	Date Filed	Title	Inventor Name 26
10605727	Not Issued	030	10/22/2003	METHOD FOR REDUCING SHALLOW TRENCH ISOLATION CONSUMPTION IN SEMICONDUCTOR DEVICES	DORIS, BRUCE B.
10605726	Not Issued	030	10/22/2003	METHOD AND MANUFACTURE OF THIN SILICON ON INSULATOR (SOI) WITH RECESSED CHANNEL AND DEVICES MANUFACTURED THEREBY	DORIS, BRUCE B.
10605697	Not Issued	041	10/21/2003	GATE STRUCTURE WITH INDEPENDENTLY TAILORED VERTICAL DOPING PROFILE	DORIS, BRUCE B.
10605672	Not Issued	071	10/16/2003	HIGH PERFORMANCE STRAINED CMOS DEVICES	DORIS, BRUCE B.
10605130	Not Issued	030	09/10/2003	STRUCTURE AND METHOD FOR SILICIDED METAL GATE TRANSISTORS	DORIS, BRUCE B.
10604907	Not Issued	030	08/26/2003	THIN CHANNEL FET WITH RECESSED SOURCE/DRAINS AND EXTENSIONS	DORIS, BRUCE B.
10604382	Not Issued	093	07/16/2003	ULTRA-THIN CHANNEL DEVICE WITH RAISED SOURCE AND DRAIN AND SOLID SOURCE EXTENSION DOPING	DORIS, BRUCE B.
10604196	Not Issued	030	06/30/2003	METHODS OF PLANARIZATION	DORIS, BRUCE
10604097	Not Issued	030	06/26/2003	HYBRID PLANAR AND FINFET CMOS DEVICES	DORIS, BRUCE B.
10437370	Not Issued	030	05/13/2003	STRUCTURE AND METHOD TO PRESERVE STI DURING ETCHING	DORIS, BRUCE B.
10375608	Not Issued	030	02/27/2003	ANTI-SPACER STRUCTURE FOR IMPROVED GATE ACTIVATION	DORIS, BRUCE B.

10345472	Not Issued	095	01/15/2003	LOW-GIDL MOSFET STRUCTURE AND METHOD FOR FABRICATION	DORIS, BRUCE B.
10342423	Not Issued	094	01/14/2003	DAMASCENE METHOD FOR IMPROVED MOS TRANSISTOR	DORIS, BRUCE B.
10338930	6780694	150	01/08/2003	MOS TRANSISTOR	DORIS, BRUCE B.
10338071	6764883	150	01/07/2003	AMORPHOUS AND POLYCRYSTALLINE SILICON NANOLAMINATE	DORIS, BRUCE B.
10328234	Not Issued	090	12/23/2002	SELF-ALIGNED PLANAR DOUBLE-GATE PROCESS BY AMORPHIZATION	DORIS, BRUCE B.
10318602	Not Issued	092	12/12/2002	STRESS INDUCING SPACERS	DORIS, BRUCE B.
10318601	6717216	150	12/12/2002	FIELD EFFECT TRANSISTOR WITH STRESSED CHANNEL AND METHOD FOR MAKING SAME	DORIS, BRUCE B.
10318600	Not Issued	041	12/12/2002	ISOLATION STRUCTURES FOR IMPOSING STRESS PATTERNS	DORIS, BRUCE B.
10304163	Not Issued	094	11/25/2002	CMOS DEVICE STRUCTURE WITH IMPROVED PFET GATE ELECTRODE	DORIS, BRUCE B.
10250241	Not Issued	030	06/17/2003	HIGH-PERFORMANCE CMOS SOI DEVICES ON HYBRID CRYSTAL-ORIENTED SUBSTRATES	DORIS, BRUCE B.
10250069	Not Issued	061	06/02/2003	STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES	DORIS, BRUCE B.
10250053	Not Issued	071	05/30/2003	METHOD OF FABRICATING SHALLOW TRENCH ISOLATION BY ULTRA-THIN SIMOX PROCESSING	DORIS, BRUCE B.
10250047	Not Issued	093	05/30/2003	STI STRESS MODIFICATION BY NITROGEN PLASMA TREATMENT FOR IMPROVING PERFORMANCE IN SMALL WIDTH DEVICES	DORIS, BRUCE B.
10249296	6790733	150	03/28/2003	PRESERVING TEOS HARD MASK USING COR FOR RAISED SOURCE-DRAIN INCLUDING REMOVABLE/DISPOSABLE SPACER	DORIS, BRUCE B.

08172974	5383354	150	12/27/1993	PROCESS FOR MEASURING SURFACE TOPOGRAPHY USING ATOMIC FORCE MICROSCOPY	DORIS , BRUCE B.

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Inventor Name Search Result

Your Search was:

Last Name = BOYD
First Name = DIANE

Application#	Patent#	Status	Date Filed	Title	Inventor Name 28
10795672	Not Issued	030	03/08/2004	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	BOYD, DIANE C.
10786901	Not Issued	030	02/25/2004	CMOS SILICIDE METAL GATE INTEGRATION	BOYD, DIANE C.
10725849	Not Issued	030	12/02/2003	ULTRA-THIN SI CHANNEL MOSFET USING A SELF-ALIGNED OXYGEN IMPLANT AND DAMASCENE TECHNIQUE	BOYD, DIANE C.
10725848	Not Issued	030	12/02/2003	ULTRA-THIN SI MOSFET DEVICE STRUCTURE AND METHOD OF MANUFACTURE	BOYD, DIANE C.
10710736	Not Issued	019	01/01/0001	ULTRA-THIN BODY SUPER-STEEP RETROGRADE WELL (SSRW) FET DEVICES	BOYD, DIANE C.
10710272	Not Issued	019	01/01/0001	METHOD AND STRUCTURE FOR STRAINED FINFET DEVICES	BOYD, DIANE C.
10707018	Not Issued	030	11/14/2003	STRESSED SEMICONDUCTOR DEVICE STRUCTURES HAVING GRANULAR SEMICONDUCTOR MATERIAL	BOYD, DIANE C.
10605889	Not Issued	041	11/04/2003	OXIDATION METHOD FOR ALTERING A FILM STRUCTURE AND CMOS TRANSISTOR STRUCTURE FORMED THEREWITH	BOYD, DIANE C.
10604097	Not Issued	030	06/26/2003	HYBRID PLANAR AND FINFET CMOS DEVICES	BOYD, DIANE C.
10461821	Not Issued	071	06/13/2003	FULLY-DEPLETED SOI MOSFETS WITH LOW SOURCE AND DRAIN RESISTANCE AND	BOYD, DIANE C.

				MINIMAL OVERLAP CAPACITANCE USING A RECESSED CHANNEL DAMASCENE GATE PROCESS	
10300165	Not Issued	071	11/20/2002	METHOD AND PROCESS TO MAKE MULTIPLE-THRESHOLD METAL GATES CMOS TECHNOLOGY	BOYD, DIANE C.
10202329	Not Issued	092	07/24/2002	SOI WAFERS WITH 30-100 A BURIED OXIDE (BOX) CREATED BY WAFER BONDING USING 30-100 A THIN OXIDE AS BONDING LAYER	BOYD, DIANE C.
10127196	6762469	150	04/19/2002	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	BOYD, DIANE C.
10084550	6660598	150	02/26/2002	METHOD OF FORMING A FULLY-DEPLETED SOI (SILICON-ON-INSULATOR) MOSFET HAVING A THINNED CHANNEL REGION	BOYD, DIANE C.
09866239	6353249	150	05/25/2001	MOSFET WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR AND MINIMUM OVERLAP CAPACITANCE	BOYD, DIANE CATHERINE
09672185	6440808	150	09/28/2000	DAMASCENE-GATE PROCESS FOR THE FABRICATION OF MOSFET DEVICES WITH MINIMUM POLY-GATE DEPLETION, SILICIDED SOURCE AND DRAIN JUNCTIONS, AND LOW SHEET RESISTANCE GATE-POLY	BOYD, DIANE CATHERINE
09503926	6271094	150	02/14/2000	METHOD OF MAKING MOSFET WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR AND MINIMUM OVERLAP CAPACITANCE	BOYD, DIANE CATHERINE
09488806	6245619	150	01/21/2000	DISPOSABLE-SPACER DAMASCENE-GATE PROCESS FOR SUB 0.05 MN. MOS DEVICES	BOYD, DIANE CATHERINE
09374519	6143635	150	08/16/1999	FIELD EFFECT TRANSISTORS WITH IMPROVED IMPLANTS AND METHOD FOR MAKING SUCH TRANSISTORS	BOYD , DIANE C.
09299137	6461529	150	04/26/1999	ANISOTROPIC NITRIDE ETCH	BOYD , DIANE

				PROCESS WITH HIGH SELECTIVITY TO OXIDE AND PHOTORESIST LAYERS IN A DAMASCENE ETCH SCHEME	C.
09192137	6221562	150	11/13/1998	RESIST IMAGE REVERSAL BY MEANS OF SPUN-ON-GLASS	BOYD , DIANE C.
09082886	6014422	250	05/21/1998	NOVEL METHOD FOR VARYING X-RAY HYBRID RESIST SPACE DIMENSIONS	BOYD , DIANE C.
09026261	6040214	150	02/19/1998	METHOD FOR MAKING FIELD EFFECT TRANSISTORS HAVING SUB-LITHOGRAPHIC GATES WITH VERTICAL SIDE WALLS	BOYD , DIANE C.
09026094	Not Issued	161	02/19/1998	FIELD EFFECT TRANSISTORS WITH IMPROVED IMPLANTS AND METHOD FOR MAKING SUCH TRANSISTORS	BOYD , DIANE C.
09026093	6593617	150	02/19/1998	FIELD EFFECT TRANSISTORS WITH VERTICAL GATE SIDE WALLS AND METHOD FOR MAKING SUCH TRANSISTORS	BOYD , DIANE C.
07786589	5299989	150	11/01/1991	ALL SURFACE TRAMPOLINE	BOYD , DIANE J.
07730482	Not Issued	161	07/16/1991	ALL SURFACE TRAMPOLINE	BOYD , DIANE J.
07593652	Not Issued	161	10/03/1990	TRAMPOLINES	BOYD , DIANE

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Inventor Name Search Result

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Last Name = IEONG
First Name = MEIKEI

Application#	Patent#	Status	Date Filed	Title	Invent Name
60534916	Not Issued	020	01/07/2004	ENHANCEMENT OF ELECTRON AND HOLE MOBILITIES IN <110> SI UNDER BIAXIAL COMPRESSIVE STRAIN	IEONG MEIKI
10876155	Not Issued	020	06/24/2004	INTEGRATION OF STRAINED GE INTO ADVANCED CMOS TECHNOLOGY	IEONG MEIKI
10872605	Not Issued	020	06/21/2004	HYBRID SUBSTRATE TECHNOLOGY FOR HIGH-MOBILITY PLANAR AND MULTIPLE-GATE MOSFETS	IEONG MEIKI
10862073	Not Issued	020	06/04/2004	STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES	IEONG MEIKI
10830347	Not Issued	020	04/22/2004	STRAINED SILICON CMOS ON HYBRID CRYSTAL ORIENTATIONS	IEONG MEIKI
10799380	Not Issued	030	03/12/2004	CMOS ON HYBRID SUBSTRATE WITH DIFFERENT CRYSTAL ORIENTATIONS USING SILICON-TO-SILICON DIRECT WAFER BONDING	IEONG MEIKI
10795672	Not Issued	030	03/08/2004	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	IEONG MEIKI
10732322	Not Issued	030	12/10/2003	SECTIONAL FIELD EFFECT DEVICES AND METHOD OF FABRICATION	IEONG MEIKI
10725849	Not Issued	030	12/02/2003	ULTRA-THIN SI CHANNEL MOSFET USING A SELF-ALIGNED OXYGEN IMPLANT AND DAMASCENE TECHNIQUE	IEONG MEIKI
10725848	Not Issued	030	12/02/2003	ULTRA-THIN SI MOSFET DEVICE STRUCTURE AND METHOD OF MANUFACTURE	IEONG MEIKI
10713971	Not Issued	030	11/14/2003	METHOD AND STRUCTURE OF A DISPOSABLE REVERSED SPACER PROCESS FOR HIGH PERFORMANCE RECESSED CHANNEL CMOS	IEONG MEIKI
10710736	Not Issued	019	01/01/0001	ULTRA-THIN BODY SUPER-STEEP RETROGRADE WELL (SSRW) FET DEVICES	IEONG MEIKI
10710277	Not	020	06/30/2004	STRUCTURE AND METHOD FOR	IEONG

	Issued			MANUFACTURING PLANAR SOI SUBSTRATE WITH MULTIPLE ORIENTATIONS	MEIKI
10710273	Not Issued	020	06/30/2004	ULTRA THIN BODY FULLY-DEPLETED SOI MOSFETS	IEONG MEIKI
10696634	Not Issued	041	10/29/2003	CMOS ON HYBRID SUBSTRATE WITH DIFFERENT CRYSTAL ORIENTATIONS USING SILICON-TO-SILICON DIRECT WAFER BONDING	IEONG MEIKI
10674644	Not Issued	094	09/30/2003	THREE DIMENSIONAL CMOS INTEGRATED CIRCUITS HAVING DEVICE LAYERS BUILT ON DIFFERENT CRYSTAL ORIENTED WAFERS	IEONG MEIKI
10669898	Not Issued	030	09/24/2003	METHOD AND APPARATUS FOR FABRICATING CMOS FIELD EFFECT TRANSISTORS	IEONG MEIKI
10663471	Not Issued	030	09/15/2003	SELF-ALIGNED PLANAR DOUBLE-GATE PROCESS BY SELF-ALIGNED OXIDATION	IEONG MEIKI
10650229	Not Issued	030	08/28/2003	ULTRA THIN CHANNEL MOSFET	IEONG MEIKI
10647395	Not Issued	093	08/25/2003	ULTRA-THIN SILICON-ON-INSULATOR AND STRAINED-SILICON-DIRECT-ON-INSULATOR WITH HYBRID CRYSTAL ORIENTATIONS	IEONG MEIKI
10634446	Not Issued	092	08/05/2003	SELF-ALIGNED SOI WITH DIFFERENT CRYSTAL ORIENTATION USING WAFER BONDING AND SIMOX PROCESSES	IEONG MEIKI
10604097	Not Issued	030	06/26/2003	HYBRID PLANAR AND FINFET CMOS DEVICES	IEONG MEIKI
10328285	Not Issued	041	12/23/2002	SELF-ALIGNED ISOLATION DOUBLE-GATE FET	IEONG MEIKI
10328234	Not Issued	090	12/23/2002	SELF-ALIGNED PLANAR DOUBLE-GATE PROCESS BY AMORPHIZATION	IEONG MEIKI
10250241	Not Issued	030	06/17/2003	HIGH-PERFORMANCE CMOS SOI DEVICES ON HYBRID CRYSTAL-ORIENTED SUBSTRATES	IEONG MEIKI
10250069	Not Issued	061	06/02/2003	STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES	IEONG MEIKI
10242941	Not Issued	164	09/13/2002	VARIABLE THRESHOLD VOLTAGE DOUBLE GATED TRANSISTORS	IEONG MEIKI
10127196	6762469	150	04/19/2002	HIGH PERFORMANCE CMOS DEVICE STRUCTURE WITH MID-GAP METAL GATE	IEONG MEIKI
10117959	6677646	150	04/05/2002	METHOD AND STRUCTURE OF A DISPOSABLE REVERSED SPACER PROCESS FOR HIGH PERFORMANCE RECESSED CHANNEL CMOS	IEONG MEIKI
09972172	6492212	150	10/05/2001	VARIABLE THRESHOLD VOLTAGE DOUBLE GATED TRANSISTORS AND METHOD OF	IEONG MEIKI

				FABRICATION	
09886823	Not Issued	041	06/21/2001	DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION	IEONG MEIKE
09886681	Not Issued	161	06/21/2001	MOSFET HAVING A VARIABLE GATE OXIDE THICKNESS AND A VARIABLE GATE WORK FUNCTION, AND A METHOD FOR MAKING THE SAME	IEONG MEIKE
09866239	6353249	150	05/25/2001	MOSFET WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR AND MINIMUM OVERLAP CAPACITANCE	IEONG MEIKE
09503926	6271094	150	02/14/2000	METHOD OF MAKING MOSFET WITH HIGH DIELECTRIC CONSTANT GATE INSULATOR AND MINIMUM OVERLAP CAPACITANCE	IEONG MEIKE

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Last Name = KANARSKY
First Name = THOMAS

Application#	Patent#	Status	Date Filed	Title	Inventor Name 21
10862073	Not Issued	020	06/04/2004	STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES	KANARSKY, THOMAS S.
10732322	Not Issued	030	12/10/2003	SECTIONAL FIELD EFFECT DEVICES AND METHOD OF FABRICATION	KANARSKY, THOMAS SAFRON
10713971	Not Issued	030	11/14/2003	METHOD AND STRUCTURE OF A DISPOSABLE REVERSED SPACER PROCESS FOR HIGH PERFORMANCE RECESSED CHANNEL CMOS	KANARSKY, THOMAS S.
10650229	Not Issued	030	08/28/2003	ULTRA THIN CHANNEL MOSFET	KANARSKY, THOMAS S.
10604097	Not Issued	030	06/26/2003	HYBRID PLANAR AND FINFET CMOS DEVICES	KANARSKY, THOMAS S.
10300165	Not Issued	071	11/20/2002	METHOD AND PROCESS TO MAKE MULTIPLE-THRESHOLD METAL GATES CMOS TECHNOLOGY	KANARSKY, THOMAS S.
10250069	Not Issued	061	06/02/2003	STRUCTURE AND METHOD TO FABRICATE ULTRA-THIN SI CHANNEL DEVICES	KANARSKY, THOMAS S.
10117959	6677646	150	04/05/2002	METHOD AND STRUCTURE OF A DISPOSABLE REVERSED SPACER PROCESS FOR HIGH PERFORMANCE RECESSED CHANNEL CMOS	KANARSKY, THOMAS S.
09824896	Not Issued	161	04/03/2001	PROCESS OF MANUFACTURING A DYNAMIC RANDOM ACCESS MEMORY DEVICE	KANARSKY, THOMAS S.
09765562	Not Issued	161	01/19/2001	METHOD OF FORMING A BURIED BITLINE IN A	KANARSKY, THOMAS

				VERTICAL DRAM DEVICE	SAFRON
09702338	6583462	150	10/31/2000	VERTICAL DRAM HAVING METALLIC NODE CONDUCTOR	KANARSKY, THOMAS
09651614	6258661	150	08/30/2000	FORMATION OF OUT-DIFFUSED BITLINE BY LASER ANNEAL	KANARSKY, THOMAS S.
09394964	6333533	150	09/10/1999	TRENCH STORAGE DRAM CELL WITH VERTICAL THREE-SIDED TRANSFER DEVICE	KANARSKY , THOMAS S.
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09138442	6238589	150	08/21/1998	METHODS FOR MONITORING COMPONENTS IN THE TIW ETCHING BATH USED IN THE FABRICATION OF C4S	KANARSKY , THOMAS SAFRON
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08740569	5759437	150	10/31/1996	ETCHING OF TI-W FOR C4 REWORK	KANARSKY , THOMAS S.
08711433	5796168	150	09/06/1996	METALLIC INTERCONNECT PAD AND INTEGRATED CIRCUIT STRUCTURE USING SAME WITH REDUCED UNDERCUT	KANARSKY , THOMAS S.
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08460439	5536388	150	06/02/1995	VERTICAL ELECTROETCH TOOL NOZZLE AND METHOD	KANARSKY , THOMAS S.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name 7
10786901	Not Issued	030	02/25/2004	CMOS SILICIDE METAL GATE INTEGRATION	KEDZIERSKI, JAKUB T
10732322	Not Issued	030	12/10/2003	SECTIONAL FIELD EFFECT DEVICES AND METHOD OF FABRICATION	KEDZIERSKI, JAKUB TADEUSZ
10725851	Not Issued	030	12/02/2003	METHOD FOR INTEGRATION OF SILICIDE CONTACTS AND SILICIDE GATE METALS	KEDZIERSKI, JAKUB T.
10669898	Not Issued	030	09/24/2003	METHOD AND APPARATUS FOR FABRICATING CMOS FIELD EFFECT TRANSISTORS	KEDZIERSKI, JAKUB T.
10604097	Not Issued	030	06/26/2003	HYBRID PLANAR AND FINFET CMOS DEVICES	KEDZIERSKI, JAKUB T
10300165	Not Issued	071	11/20/2002	METHOD AND PROCESS TO MAKE MULTIPLE-THRESHOLD METAL GATES CMOS TECHNOLOGY	KEDZIERSKI, JAKUB TADEUSZ
09695532	6413802	150	10/23/2000	FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE	KEDZIERSKI, JAKUB TADEUSZ

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